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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SUGENT, JAMES F	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/764,406	NEWMAN, PAUL F.	
	Examiner	Art Unit	
	James F. Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-11,13-18,20-22 and 28-32* is/are rejected.

7)☒ Claim(s) *20 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is sent in response to Applicant's Communication received June 30, 2006 for application number 10/764406 originally filed January 23, 2004. The Office hereby acknowledges receipt of the following and placed of record in file: amended claims 1-32 wherein claims 5, 12, 19 and 23-27 have been cancelled and claims 28-32 are new.

Claim Objections

Claims 20 and 32 are objected to because of the following informalities:

- Claim 20 recites, "The system according to claim 19, wherein..." on line 1 of claim 20 wherein claim 19 has been canceled by the Applicant. The Examiner asserts Applicant overlooked the dependence when canceling claim and the Applicant's intention was to have claim 20 now dependent upon claim 18. Please change "The system according to claim 19, wherein..." to read "The system according to claim 18, wherein..."
- Claim 32 recites, "...wherein the the delay element..." on line 4 of claim 32. Please change to "...wherein the delay element..."

Appropriate correction is required.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 6-11, 13-18, 20-22 and 28-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Ovens et al. (U.S. Patent No. 6,351,173 B1) (hereinafter referred to as Ovens).

As to claim 1, Ovens discloses an apparatus, comprising: a clock source (clock tree synthesis circuit, not shown in Ovens, and hereinafter referred to as CTS) to generate a clock signal (clock signals 114 and 116 in core 104); a first circuit (core), coupled to a first supply voltage source (V_{DD}), to generate a first data signal (D 120) and a second circuit (I/O) coupled to a second supply voltage source (V_{DDS}) (column 3, lines 43-61); a flip-flop (118; column 3, lines 31-32), having a pair of inputs coupled to the clock source (CLKT and CLKF) and the first circuit, to generate a second data signal (Q 122 in Box B of core 104) in response to the clock signal and the first data signal (column 3, lines 31-32 and column 3, lines 62-66); a first level shifter (126), coupled to the flip-flop (as shown in fig. 1), to generate a level shifted data signal (Y 128) in response to the second data signal (column 3, line 66 thru column 4, line 2); a delay element (not shown in 108) coupled to the clock source and responsive to the clock signal to generate a delayed clock signal having a triggering clock edge (column 3, lines 43-61); and, a downstream latch (transmission gate between lines N4 and N7), having an open state and a close state (as is inherent to transmission gates), a pair of inputs coupled to the first level shifter and the delay element and an output coupled to the second circuit (as shown in fig. 1), to generate an output data signal (Y 128) in response to the level shifted data signal and the delayed clock signal, with the triggering clock edge of the delayed clock signal switching the downstream latch from the close state to the open state (via CLKT and CLKF) (column 3, line 51 thru column 4, line 19).

As to claim 2, Ovens further discloses the apparatus further comprising: a second level shifter (clock level shifter 108), coupled between the clock source and the downstream latch and in series with the delay element (column 3, lines 43-61).

As to claim 3, it is directed to the apparatus of steps set forth in claims 1 and 2. Therefore, it is rejected for the same basis as set forth hereinabove.

As to claim 4, Ovens further discloses the apparatus wherein the delayed clock signal has a plurality of clock cycles (CLKT and CLKF) with each of the clock cycles having a rising clock edge and a falling clock edge; and, the downstream latch (transmission gate) is switched from the close state to the open state (as is inherent to transmission gates) by the triggering clock edge selected from the rising clock edge and the falling clock edge (as shown in fig. 1) and switched from the open state to a close state by the non-selected clock edge of the rising clock edge and the falling clock edge (column 3, line 43 thru column 4, line 19).

As to claims 6-9, they are directed to the apparatus of steps set forth in claims 1 and 4. Therefore, they are rejected for the same basis as set forth hereinabove.

As to claim 10, Ovens discloses an apparatus, comprising: a microprocessor including a central processing unit (CPU) section (fig. 1) having a first supply voltage source (V_{DD}); an input-output (I/O) section (fig. 1) having a second supply voltage source (V_{DDS}) (column 3, lines 43-61); a clock source (clock tree synthesis circuit, not shown in Ovens, and hereinafter referred to as CTS) to generate a clock signal (clock signals 114 and 116 in core 104); and a selected section (not shown) of the CPU section and the I/O sections being operable to generate a first data signal (D 120), with the selected section providing a first data signal (column 3, lines 43-61); a converter circuit (fig. 1) including a flip-flop (118; column 3, lines 31-32), coupled to the

clock source and the selected section (as shown in fig. 1), to generate a second data signal (Q 122) in response to the clock signal and the first data signal (column 3, line 66 thru column 4, line 2); a first level shifter (126), coupled to the selected section, to generate a level shifted data signal (Y 128) in response to the second data signal (column 3, line 66 thru column 4, line 2); a delay element (not shown in 108) and a second level shifter, coupled in series to the clock source, to generate a level shifted clock signal with a triggering clock edge in response to the clock signal (column 3, lines 43-61); a downstream latch (transmission gate between lines N4 and N7) having an open and close state (as is inherent to transmission gates), a pair of inputs coupled to the first level shifter and the series-coupled delay element and second level shifter, and an output (Y 128) coupled to the non-selected section of the CPU and I/O sections (as shown in fig. 1); and, the downstream latch adapted to generate an output data signal (Y 128) in response to the level shifted data signal and the triggering clock edge of the level shifted clock signal (column 3, line 51 thru column 4, line 19).

As to claim 11, Ovens further discloses the apparatus wherein the level shifted clock signal has a plurality of clock cycles (CLKT and CLKF) with each of the clock cycles having a rising clock edge and a falling clock edge; the downstream latch (transmission gate) has an open and a close state (as is inherent to transmission gates); and the downstream latch is switched from the close state to the open state by the triggering clock edge selected from the rising clock edge and the falling clock edge (column 3, line 43 thru column 4, line 19).

As to claims 13-15, they are directed to the apparatus of steps set forth in claims 10 and 11. Therefore, they are rejected for the same basis as set forth hereinabove.

As to claim 16, Ovens discloses a system, comprising: a microprocessor including a central processing unit (CPU) section (fig. 1) coupled to a first supply voltage source (V_{DD}); an input-output (I/O) section (fig. 1) coupled to a second supply voltage source (V_{DDS}) (column 3, lines 43-61); a clock source (clock tree synthesis circuit, not shown in Ovens, and hereinafter referred to as CTS) to generate a clock signal (clock signals 114 and 116 in core 104); and the CPU section being operable to generate a first data signal (D 120) (column 3, lines 43-61); a converter circuit (fig. 1) including a flip-flop (118; column 3, lines 31-32), coupled to the clock source and the selected section (as shown in fig. 1), to generate a second data signal (Q 122) in response to the clock signal and the first data signal (column 3, line 66 thru column 4, line 2); a first level shifter (126), coupled to the CPU section, to generate a level shifted data signal (Y 128) in response to the second data signal (column 3, line 66 thru column 4, line 2); a delay element (not shown in 108) and a second level shifter, coupled in series to the clock source, to generate a level shifted clock signal having a triggering clock edge in response to the clock signal (column 3, lines 43-61); and a downstream latch (transmission gate between lines N4 and N7) having an open and close state (as is inherent to transmission gates), a pair of inputs coupled to the first and second level shifters and an output (Y 128) coupled to the I/O section (as shown in fig. 1); the downstream latch being adapted to generate an output data signal (Y 128) in response to the level shifted data signal and the triggering clock edge of the level shifted clock signal (column 3, line 51 thru column 4, line 19); a source synchronous bus, coupled to the I/O section, to receive the level shifted data signal and the level shifted clock signal (Ovens discloses the level shifting circuit being part of an integrated circuit [microprocessor] wherein, as is known in the art, is coupled at the I/O pins to a bus to transfer said data/clock signals for

synchronization of processing; column 1, lines 11-23); and an I/O module coupled to the source synchronous bus (Though an I/O module is not explicitly stated, Ovens does disclose the output Y 128 of the circuit in fig. 1 needing an output buffer to the output pin of the IC which necessitates the need for an I/O module wherein said output is synchronous; column 3, line 66 thru column 4, line 8 and column 2, lines 27-35).

As to claim 17, Ovens further discloses the system wherein the I/O module is a selected one of a graphics and a video controller (Ovens discloses the ICs to include programmable controllers; column 1, lines 11-24).

As to claim 18, Ovens further discloses the system wherein the level shifted clock signal has a plurality of clock cycles (CLKT and CLKF) with each of the clock cycles having a rising clock edge and a falling clock edge; the downstream latch (transmission gate) has an open and a close state (as is inherent to transmission gates); and the downstream latch is switched from the close state to open state by the triggering clock edge selected from the rising clock edge and the falling clock edge (column 3, line 43 thru column 4, line 19).

As to claims 20-22, they are directed to the system of steps set forth in claims 16 and 18. Therefore, they are rejected for the same basis as set forth hereinabove.

As to claim 28, Ovens discloses a converter circuit, comprising a flip-flop (118; column 3, lines 31-32) including a master latch (comprising N15 and N17 of fig. 1) and an upstream slave latch (transmission gate between N1 and N4), to generate a latched data signal in response to a clock signal (CLKT and/CLKF) and an input data signal (D 120) (column 3, lines 62-64 and column 3, lines 31-32); a first level shifter (126), coupled to the flip-flop (as shown in fig. 1), to generate a level shifted data signal (Y 128) in response to the latch data signal, with the level

shifted data signal having a plurality of signal transitions (column 3, line 66 thru column 4, line 2); a delay element (not shown in 108) to generate a delayed clock signal having a triggering clock edge in response to the clock signal (column 3, lines 43-61); and, a downstream slave latch (transmission gate between lines N4 and N7) having an open and a close state (as is inherent to transmission gates), coupled to the first level shifter and the delay element, to generate an output data signal (Y 128) in response to the level shifted data signal and the triggering clock edge (column 3, line 51 thru column 4, line 19).

As to claim 29, Ovens further discloses the converter circuit wherein the delay element (not shown in 108) is adapted to delay an arrival of the triggering clock edge at the downstream slave latch until after an arrival of the signal transitions at the downstream slave latch (column 3, lines 43-61).

As to claims 30 and 31, they are directed to the converter circuit of steps set forth in claims 28 and 29. Therefore, they are rejected for the same basis as set forth hereinabove.

As to claim 32, Ovens further discloses the converter circuit further comprising: a second level shifter (clock level shifter 108), coupled in series with the delay element, to voltage level shift the delayed clock signal (column 3, lines 43-50); and, wherein the delay element is adapted to introduce a predetermined delay having a duration exceeding a time period during which the rising and falling data edges are mismatched (column 3, lines 43-61).

Response to Arguments

Applicant's arguments with respect to claims 1-32 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The Examiner can normally be reached on 8AM - 4PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or (571) 272-1000.

James F. Sugent
Patent Examiner, Art Unit 2116
September 5, 2006

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PRIMARY EXAMINER
TC 2100